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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/844,671	04/30/2001	Radhika Thekkath	MTEC002/00US (0119.00US)	8986

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EXAMINER	
SHAAWAT, MUSSA	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 11/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/844,671	THEKKATH ET AL.	
	Examiner	Art Unit	
	Mussa A Shaawat	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *30 April 2001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is responsive to application # 09/844,671, filed on April 30 2001. Claims 1-21 are presented for examination.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) The invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-21 are rejected under 35 U.S.C. 102(e) as being anticipated by James M. Torrey US Patent No. (6,145,123) referred to hereinafter as Torrey.

Re claims 1, Torrey teaches a method for tracing instructions in a microprocessor core that supports execution of instructions in a plurality of instruction pipelines, comprising: holding trace data for one or more instructions in a group of instructions that were issued together until all instructions in said group of instructions should complete (see figure 5 [530–590] the microprocessor executes all the instructions by checking the LAST INSTRUCTION at block [590] to determine if it is the last instruction; otherwise it loops back and execute the next instruction in the group at block [530]); and transmitting trace data for said group of instructions along with information that enables a determination of a static schedule of said group of instructions (see col.5 lines 29-32, and col.6 lines 31-45).

Re claims 2, Torrey teaches a method of claim 1, wherein in an instruction pipeline having a fetch stage (see col.8 lines 49-50), a processor 110 to execute the instruction, which

must (inherently) include a decoder stage to read the instruction (see col. 9 lines 56-58), an execute stage (see Abstract line 5), a memory stage (see col.1 lines 26-27), an align stage (see col.8 lines 40-41), and a write back stage (see col.6 lines 31-34), an instruction should complete after said memory stage (see col.8 lines 55-57, when processor 110 completes the execution of an instruction it stores it in memory 120).

Re claims 3, Torrey teaches a method of claim 1, wherein said transmitting comprises transmitting information that enables a determination of a static schedule position of a first instruction in said group of instructions (see col.4 lines 8-27).

Re claims 4, Torrey teaches a method of claim 3, wherein said transmitting comprises transmitting a program order signal for each of said plurality of instruction pipelines (see col.5 lines 51-55, col.6 lines 10-14, and col.10 lines 35-37).

Re claims 5, Torrey teaches a method of claim 4, wherein said program order signal includes a multi-bit signal (see col.10 lines 35-37)

Re claims 6, Torrey teaches a method of claim 5, wherein said multi-bit signal identifies a static schedule position for an instruction in a group of instructions (see col.4 lines 8-27).

Re claims 7, Torrey teaches a method of claim 1, wherein said trace data includes program counter information (see col.1 lines 39-40).

Re claims 8, Torrey teaches a method of claim 1, wherein said trace data also includes one or more of load address, load data, store address, and store data information (see col.3 lines 63-67, a microprocessor includes a breakpoint register with the ability to receive and store address, which inherently teaches loading, storing, receiving address and data information).

Re Claims 9-16, the limitations of claims 9-16 are similar to the limitations of claims 1-8; therefore they are rejected based on the same rationale, supra.

Re claims 17, Torrey teaches a computer program product comprising: computer-readable program code for causing a computer to describe a buffer configured to store trace data for one or more instructions in a group of instructions that were issued together, said buffer holding said trace data until all instructions in said group of instructions should complete (see Abstract lines 1-11); and computer-readable program code for causing a computer to describe a trace generation module that transmits trace data for said group of instructions along with information that enables a determination of a static schedule of said group of instructions; and a computer-usable medium configured to store the computer-readable program codes (see Abstract lines 12-18, and col.5 lines 29-32).

Re claims 18, Torrey teaches a method for enabling a computer to generate tracing logic, comprising: transmitting computer-readable program code to a computer, said computer-readable program code including: computer-readable program code for causing a computer to describe a buffer configured to store trace data for one or more instructions in a group of instructions that were issued together, said buffer holding said trace data until all instructions in said group of instructions should complete (see Abstract lines 1-11); and computer-readable program code for causing a computer to describe a trace generation module that transmits trace data for said group of instructions along with information that enables a determination of a static schedule of said group of instructions (see Abstract lines 12-18, and col.5 lines 29-32).

Re claims 19, Torrey teaches a method of claim 18, wherein computer-readable program code is transmitted to said computer over the Internet (see col.5 lines 35-38).

Re claims 20, Torrey teaches a computer data signal embodied in a transmission medium comprising: computer-readable program code for causing a computer to describe a buffer configured to store trace data for one or more instructions in a group of instructions that were issued together, said buffer holding said trace data until all instructions in said group of instructions should complete (see Abstract lines 1-11); and computer-readable program code for causing a computer to describe a trace generation module that transmits trace data for said group of instructions along with information that enables a determination of a static schedule of said group of instructions (see Abstract lines 12-18, and col.5 lines 29-32).

Re claims 21, Torrey teaches a method for tracing instructions in a microprocessor core that supports execution of instructions in a plurality of instruction pipelines, comprising: generating trace data that is associated with a plurality of instructions having a program order, each of said plurality of instructions being executed by one of a plurality of instruction pipelines, wherein said generated trace data includes program order information that enables a trace capture component to determine a relative order between instructions that were completed out of order by respective instruction pipelines (see Abstract lines 12-18, and col.5 lines 29-32).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Kurkooka et al. US Patent No. (6,813,732)
- Bortfeld US Patent No. (6,718,294) system and method for synchronized control of system simulators with multiple process cores.

- Deao et al. US Patent No. (6,112,298) Method for managing an instruction execution pipeline during debugging of a data processing system.

Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mussa A Shaawat whose telephone number is (571) 272-3785. The examiner can normally be reached on Monday-Friday (8:30am to 5:00pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean R Homere can be reached on (571) 272-3780. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mussa Shaawat
Patent Examiner
November 9, 2004

JEAN R. HOMERE
PRIMARY EXAMINER